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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,643	12/17/2003	Michael A. Kneissl	115255	3827

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,643	KNEISSL ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11,13,15,16,18,21 and 23* is/are rejected.

7)☒ Claim(s) *3,12,14,17,19,20,22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 04/16/2004 is acceptable.

Drawings

2. The formal drawings filed on 12/17/2003 are acceptable.

Priority

3. Applicants have made no claim for priority.

Information Disclosure Statement

4. The Information Disclosure Statement filed on 03/10/2006 has been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1,2,4,8,10,11, and 13 stand rejected under 35 U.S.C. 102(b) as being anticipated by SAITO ET AL. (6,121,63).

Saito et al. discloses a semiconductor laser diode comprising a GaN, InGaN, AlGaN, or InAlGaN multiple quantum well (said multiple quantum well comprising undoped barrier layers) active region 205 having a thickness of about 9 nm, a p-side, and an n-side; an n-type Si doped carrier confinement layer 207 provided on the n-side of the single or multiple quantum well active region 205; a p-type Mg doped carrier confinement layer 203 provided on the p-side of the single or multiple quantum well active region 205; and undoped spacer layers 204,206 provided between the single or multiple quantum well active region 205 and the n-type 207 and p-type 203 carrier confinement layers; barriers between quantum wells in the multiple quantum well active region 205 having a thickness between about 1 nm and about 10 nm. Note figures 6A and column 8 line 16 through column 9 line 4 of Saito et al.

B. Claims 1,2,5-7,9-11,16,18,21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by MATSUMOTO ET AL. (EP908988A).

Matsumoto et al. discloses a semiconductor laser diode comprising a GaN, InGaN, AlGaN, or InAlGaN multiple quantum well (said multiple quantum well comprising undoped barrier layers) active region 607 having a p-side and an n-side; an n-type Si doped carrier confinement layer 605 provided on the n-side of the single or multiple quantum well active region 607; a p-type Mg doped carrier confinement layer 609

provided on the p-side of the single or multiple quantum well active region 607; undoped spacer layers 606,608 provided between the single or multiple quantum well active region 607 and the n-type 605 and p-type 609 carrier confinement layers; a p-type waveguide layer 610 provided adjacent to the p-type carrier confinement layer 609; an n-type waveguide layer 604 provided adjacent to the n-type carrier confinement layer 605; a p-type cladding layer 611 provided adjacent to the p-type waveguide layer 610; an n-type cladding layer 603 provided adjacent to the n-type waveguide layer 604; quantum wells in the multiple quantum well active region 607 having a thickness between about 2 nm and about 20 nm; and barriers between quantum wells in the multiple quantum well active region 607 having a thickness between about 1 nm and about 10 nm; wherein an aluminum content of the p-type carrier confinement layer 609 is different than an aluminum content of the n-type carrier confinement layer 605 and the thickness (20 nm) of each of the undoped spacer layers 606,608 is about 4 nm. Note figures 11,12 and page 15 lines 5-48 of Matsumoto et al.

C. Claims 1,2,5, 8-10, and 15 stand rejected under 35 U.S.C. 102(e) as being anticipated by SEKO ET AL. (6,597,017).

Seko et al. discloses a semiconductor laser diode comprising a GaN, InGaN, AlGaN, or InAlGaN multiple quantum well active region 14 having a p-side and an n-side; an n-type carrier confinement layer 12 provided on the n-side of the single or multiple quantum well active region 14; a p-type carrier confinement layer 16 provided on the p-side of the single or multiple quantum well active region 14; and undoped spacer

layers13, 15 provided between the single or multiple quantum well active region 14 and the n-type 12 and p-type 16 carrier confinement layers; quantum wells (note column 15 lines 10-15) in the multiple quantum well active region 14 having a thickness between about 2 nm and about 20 nm.; and barriers (note column 15 lines 10-15) in the multiple quantum well active region 14 being about 6 nm thick; wherein a thickness of each undoped spacer layer 13,15 is between about 2 nm and about 20 nm. Note figure 4 and column 15 lines 1-54 of Seko et al.

Allowable Subject Matter

6. Claims 3,12,14,16,17,19,20,22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 05/10/2006 have been fully considered but they are not persuasive.

With regard to sections IIIA, IVA, and VA of his remarks, on page 2 Applicant states (correctly) "Independent claim 1 recites a III-V semiconductor laser diode that includes, inter alia, 'an n-type carrier confinement layer [emphasis added] provided on the n-side of the single or multiple quantum well active region; [and] a p-type carrier confinement layer [emphasis added] provided on the p-side of the single or multiple quantum well

active region . . .'" Applicant goes on to say, (incorrectly, unfortunately) "Saito does not include such a [p- and n-type carrier confinement layers] feature."

Applicant's argument is wholly based on his page 3 assertions that "(1) A Cladding Layer Does Not Inherently Act as a Current Confining Layer," and "(2) Saito Clearly Distinguishes Cladding Layers from Current Confining Layers."

However, Applicant's claim 1 contains no references at all to "Current Confining Layers." As Applicant correctly states, the claim refers to n-type and p-type "carrier confinement layers." There is a critical difference between the "Current Confining Layers" Saito et al.'s Cladding Layers allegedly do not act as, and the claimed "carrier confinement layers" Saito et al.'s cladding layers do, in fact, act as.

Current confining layers, such as Saito et al.'s conduction barriers 109 (figure 1A), 208 (figure 6A), 308 (figure 8), 509 (figure 13) or 709 (figure 18), act as absolute barriers to the flow of current. Saito et al.'s figure 1A conduction barrier prevents current flow with a "double junction," by surrounding n-type barrier layer 109 with p-type layers 107 and 108. Current may flow into the barrier layer from either the top (108) or the bottom (107) but because of the two p-n junctions current may not flow out of the barrier layer, either upwardly or downwardly. Consequently no current may flow. Saito et al.'s figures 6A and 8 conduction barriers prevent current flow with a "double junction," by surrounding p-type barrier layer 208/308 with n-type layers 207/307 and 209/309. Current may flow out of these p-type barrier layers into either the top (209/309) or the

bottom (207/307) but because of the two n-p junctions current may not flow into the barrier layer, either upwardly or downwardly. Consequently no current may flow. Saito et al.'s figure 13 and 18 embodiments take a head-on approach to confining current by forming conduction barriers 509 and 709 from insulating material (silicon dioxide).

In contrast, "carrier confinement layers" (such as those formed by Saito et al.'s "cladding layers") have no objection to current flow – often they encourage it – on the sole condition that carriers of the correct type carry the current. For the past fifty years or so, scientists have generally accepted the notion that semiconductors may carry current using carriers of either a negative (when the carrier is an electron) or positive (when the carrier is a hole) charge. See, for example William Shockley, "Transistor technology evokes new physics," 12/11/1956 (Available online at http://nobelprize.org/physics/laureates/1956/shockley-lecture.pdf). As Dr. Shockley points out in his lecture, the holes naturally resident in a p-type material (such as a p-type cladding layer) tend to selectively annihilate a particular type of carrier (electrons). This process "confines" electrons in a way roughly analogous to the way a school of hungry sharks "confines" chumfish to the inside of a shark cage. In a similar way electrons, being the majority carriers in an n-type cladding layer, annihilate and thus confine holes (i.e. p-type carriers). However (and Dr. Shockley was one of the first to realize this) this process does not prevent the flow of current, because as "minority" carriers move in one direction on their way to be annihilated, oppositely charged

"majority" carriers move in the opposite direction to get into position to do the annihilating.

Simply put, a "carrier confinement layer" is not a "current confining layer," nor is a "current confining layer" a "carrier confinement layer." They are different breeds of cats.

Saito et al.'s p-type cladding layer 203 confines carriers, specifically, electrons, to active layer 205 by providing an abundance of holes to annihilate electrons that escape from active layer 205. Saito et al.'s n-type cladding layer 207 confines carriers, specifically, holes, to active layer 205 using electrons to annihilate holes that escape from active layer 205. Matsumoto et al.'s p-type cladding layer 609 confines carriers, specifically, electrons, to active layer 607 by providing an abundance of holes to annihilate electrons that escape from active layer 607. Matsumoto et al.'s n-type cladding layer 605 confines carriers, specifically, holes, to active layer 607 using electrons to annihilate holes that escape from active layer 607. Seko et al.'s p-type cladding layer 16 confines carriers, specifically, electrons, to active layer 14 by providing an abundance of holes to annihilate electrons that escape from active layer 14. Seko et al.'s n-type cladding layer 12 confines carriers, specifically, holes, to active layer 14 using electrons to annihilate holes that escape from active layer 14.

Applicant's IIIB-IIID arguments are found persuasive and the rejections of claims 3,12,19, and 21-24 over Saito et al. are withdrawn.

Applicant's IVC argument is found persuasive and the rejections of claims 12 and 19 over Matsumoto et al. are withdrawn.

It is argued, in section IVB of the remarks, that "As stated in Matsumoto at paragraph (01462, lines 4-6, non-doped guide layers 606 and 608 are about 20 nm thick. Accordingly, Matsumoto does not teach or suggest [undoped spacers about 4 nm thick]." However, spacers of this nature commonly range in thickness from a few angstroms to almost a micron. Applicants admit as much at paragraph 0053 of their spec. On this angstroms to microns scale it is safe to say that 20 nm is "about" 4nm.

Conclusion

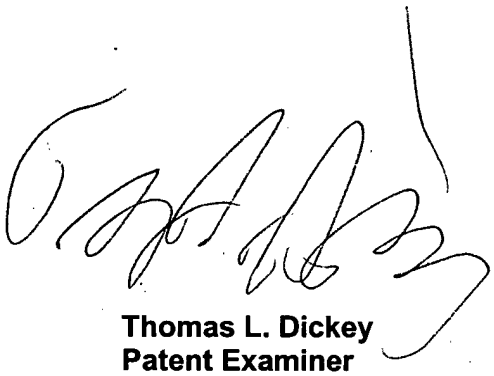
8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan

J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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05/06